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EXAMINER	
OWENS, DOUGLAS W	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/072,015	Applicant(s) RUDECK ET AL.	
	Examiner Douglas W. Owens	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-18* is/are allowed.

6)☒ Claim(s) *1-7,13 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1 – 7, 19, 20 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,194,929 to Ohshima et al.

Regarding claim 1, Ohshima et al. teach a semiconductor device (Fig. 5D) comprising:

a substrate (1);

a drain (14,19) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer;

an inter-layer insulation (5) over the first polysilicon layer;

a second polysilicon layer (6) over the inter-layer insulation; and

a phosphorous-doped oxide layer (22; Col. 8, lines 22 – 33 and lines 54 – 57) provided along substantially vertical edges of the first oxide, the first polysilicon layer, the inter-layer insulation and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. do not teach that the phosphorous-doped oxide layer is deposited. Deposition of oxide layers is known in the art, by such methods as CVD, and sputtering. It would have been obvious to one having ordinary skill in the art to

select any known method of forming the phosphorous-doped oxide layer since it is desirable to form oxide spacers using known and reliable methods. Additionally, it is desirable to form a higher quality oxide, which would have been obtained by depositing the oxide instead of thermally growing it.

Regarding claim 2, Ohshima et al. inherently teach a device, wherein the first oxide layer is a tunnel oxide layer, since that is the function of the first oxide layer of the EPROM.

Regarding claim 3, Ohshima et al. do not teach a device, wherein the inter-layer insulation is an oxide nitride oxide (ONO) layer. It is common in the art to use (ONO) layers as the inter-layer insulation film in EEPROM devices. It would have been obvious to one of ordinary skill in the art to incorporate the ONO layer, since it is desirable to use materials that are known and well suited for the intended use.

Regarding claim 4, Ohshima et al. teach a semiconductor device, wherein the first polysilicon layer is a floating gate.

Regarding claim 5, Ohshima et al. do not explicitly teach that the second polysilicon layer is used as a word line. It is common in the art to use the second polysilicon layer in this type of memory device for the word line. It would have been obvious to one of ordinary skill in the art to use the second polysilicon layer for the word line since it is desirable to produce a functioning device.

Regarding claim 6, Ohshima et al. teach a semiconductor device after re-oxidation (Col. 5, line 68 – Col. 6, line 7) comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) provided along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile formed over surfaces of the semiconductor device having a height and width, since Ohshima et al. teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Ohshima et al. do not teach that the phosphorous-doped oxide layer is deposited. Deposition of oxide layers is known in the art, by such methods as CVD, and sputtering. It would have been obvious to one having ordinary skill in the art to select any known method of forming the phosphorous-doped oxide layer since it is desirable to form oxide spacers using known and reliable methods. Additionally, it is desirable to form a higher quality oxide, which would have been obtained by depositing the oxide instead of thermally growing it.

Regarding claim 7, Ohshima et al. inherently teach a device, wherein the height is a vertical distance from the source to a bottom edge of the first polysilicon layer and the width is a horizontal distance from a side edge of the first polysilicon later to a vertical edge of the tunnel oxide layer, wherein the width is less than a re-oxidation oxide profile width without the phosphorous doped oxide, since Ohshima et al. teach the re-oxidation.

Regarding claim 19, Ohshima et al. teach a semiconductor device comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. do not teach that the phosphorous-doped oxide layer is deposited. Deposition of oxide layers is known in the art, by such methods as CVD, and sputtering. It would have been obvious to one having ordinary skill in the art to

select any known method of forming the phosphorous-doped oxide layer since it is desirable to form oxide spacers using known and reliable methods. Additionally, it is desirable to form a higher quality oxide, which would have been obtained by depositing the oxide instead of thermally growing it.

Regarding claim 20, Ohshima et al. teach a semiconductor device after re-oxidation (Col. 5, line 68 – Col. 6, line 7) comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide layer and the second polysilicon layer, the phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile having a width defined by a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide [first oxide], wherein the width is less than a re-oxidation profile width without the phosphorus doped oxide layer, since Ohshima et al.

teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Ohshima et al. do not teach that the phosphorous-doped oxide layer is deposited. Deposition of oxide layers is known in the art, by such methods as CVD, and sputtering. It would have been obvious to one having ordinary skill in the art to select any known method of forming the phosphorous-doped oxide layer since it is desirable to form oxide spacers using known and reliable methods. Additionally, it is desirable to form a higher quality oxide, which would have been obtained by depositing the oxide instead of thermally growing it.

Regarding claim 21, Ohshima et al. teach a semiconductor device after re-oxidation comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) having a first thickness and stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer, said self-aligned source extending to a point inward of an edge of the first polysilicon layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide

layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile having a width defined by a horizontal distance from a side edge of the first polysilicon layer to a point where said first oxide layer starts to get thicker than said first thickness, and a height defined by a vertical distance from a top surface of said self-aligned source to a bottom edge of said first polysilicon layer, wherein the width is less than a re-oxidation profile width and the height is higher than a re-oxidation profile height without the phosphorus doped oxide layer, since Ohshima et al. teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Ohshima et al. do not teach that the phosphorous-doped oxide layer is deposited. Deposition of oxide layers is known in the art, by such methods as CVD, and sputtering. It would have been obvious to one having ordinary skill in the art to select any known method of forming the phosphorous-doped oxide layer since it is desirable to form oxide spacers using known and reliable methods. Additionally, it is desirable to form a higher quality oxide, which would have been obtained by depositing the oxide instead of thermally growing it.

3. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohshima et al. in view of US Patent No. 6,732,241 to Riedel.

Ohshima et al. teach a flash memory device comprising:

a substrate (1);

a drain (14) formed in the substrate;

a self-aligned source (13) formed in the substrate;

a first oxide layer (3) stretching from the drain to the self-aligned source;

a first polysilicon (4) over the first oxide layer;

a second oxide layer (5) over the first polysilicon layer;

a second polysilicon layer (6) over the second oxide layer; and

a phosphorous-doped oxide (22; Col. 8, lines 22 – 33 and lines 54 – 57) along substantially vertical edges of the first oxide, the first polysilicon layer, the second oxide layer and the second polysilicon layer, said phosphorous-doped oxide layer extending no higher than the second polysilicon layer.

Ohshima et al. further inherently teach a re-oxidation profile formed over surfaces of the semiconductor device having a height and width, since Ohshima et al. teach a step that would have resulted in a re-oxidation. The profile would have been the same as disclosed by the admitted prior art.

Ohshima et al. do not teach the flash being used in a computer system comprising:

at least one processor; and

a system bus.

Riedel teaches a computer system including a processor (102) and a system bus (106), wherein the flash memory device is couple to the system bus. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Riedel into the device taught by Ohshima et al., since it is desirable to use the flash device in a functional system.

Allowable Subject Matter

4. Claims 14 – 18 are allowed.

Response to Arguments

5. Applicant's arguments with respect to claims 1 – 7, 13 and 19 – 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Douglas W Owens
Primary Examiner
Art Unit 2811

DWO
June 24, 2006